THD Minimization on the Line-to-Line Voltage of Multilevel Inverters

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Abstract— In this paper, minimization of the total harmonics (THD) present in the output voltage of multilevel inverters is discussed . In order to reduce the harmonic contents of the inverter's output voltage the best approach is THD minimization. In multilevel inverters, if fundamental frequency switching strategy is considered,(each switch turning on and off once per output cycle), the switching angles can be selected so that the output THD is minimized. To obtain the optimum switching angles, an optimization algorithm is applied to the output-voltage THD. In the case of three-phase multilevel inverters, the optimization algorithm is generally applied to the phase voltage of the inverter. This results in the minimum THD in phase voltage but not necessarily in the line-to-line minimum THD. In three-phase applications, the line-voltage harmonics are of the main concern from the load point of view. In this paper, using the genetic algorithm and sinusoidal PWM technique, a THD minimization process is applied to the line-to-line voltage of the inverter. This paper is based on a comparison between seven level cascaded and nine level diode clamped multilevel inverter.

Index Terms- Optimal minimization of THD (OMTHD), Genetic algorithm (GA), line-voltage THD, multilevel inverter, Phase Voltage THD, THD reduction..

1 INTRODUCTION

Multilevel inverters are finding increased attention in industry and academia as one of the preferred choices of electronic power conversion o high-power applications [1]-[10]. Now a days, multilevel inverters have received more attention in industrial applications, such as motor drives[1],[2], static VAR compensators (STATCOMs)[3],[4], and renewable energy systems[5]. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters. This advantage results in higher power quality, better electromagnetic compatibility, lower switching losses, higher voltage capability, and needlessness of a transformer at distribution voltage level, thereby reducing the costs [1-5]. Multilevel inverters are generally divided into three configurations: diode-clamped, flying-capacitor, and cascaded H-bridge multilevel inverters [6].

Considering the switching frequency of multilevel inverters, the strategies can be categorized into two: strategies that work with high switching frequencies and those that work with low switching frequencies, generally equal to the fundamental component frequency, and generate a staircase waveform[8]. Representatives o the first category includes the classical carrier-based sinusoidal pulse width modulation (PWM) strategy [7]. Representatives of the later are the so-called "optimized harmonic stepped waveform"[9-12], "selective harmonic mitigation PWM", and "optimal minimization of the total harmonic distortion" (THD) (OMTHD). Even though this category is not necessarily restricted to the fundamental frequency and higher switching frequencies can be employed in order to improve harmonic conditions. In this paper, fundamental frequency switching is considered. Future expansion can be made done by considering the cases with higher switching frequencies [3].

Optimal minimization of THD is an efficient method by which the switching angles are so selected such that the output harmonics should be minimum and the output voltage will be of the desired sinusoidal form. To achieve this, an optimization algorithm is employed, in which the objective is to minimize THD and either the fundamental component is considered as a constraint [16] or its error is added to the objective function[17].

Phase voltage has a unique and simple waveform so that its THD can be easily formulated [18], compared to the line-to-line voltage which changes the form as switching angles vary. Therefore, in THD minimization of a multilevel inverter's output, it is quite common to apply the minimization algorithm on the phase voltage [15],[19] . In three-phase three-wire applications, however, the inverter line-to-line voltage is of the major concern, since it determines the load-voltage harmonic contents.

In SHE techniques, the triplen harmonics are deliberately not included in the selected harmonic orders for elimination, since they will automatically be cancelled from the line-to-line voltage and, consequently, from the load phase voltage. In THD minimization methods, however, this fact is ignored, and therefore, minimization of the THD of the phase voltage does not necessary result in minimum THD in the line-to-line voltage.

In this paper, a THD minimization algorithm is applied on both phase and line-to-line voltages of the inverter, and the results are compared. According to the simulation results, there is a significant difference between the two approaches. Applying the algorithm directly on the line voltage leads to improved output voltage with less THD. The optimization algorithm used in this paper to minimize the objective function is the genetic algorithm along with sinusoidal PWM technique.

GA is a search method to find the maximum of functions by mimicking the biological evolutionary processes. There are only a few examples of GA applications for power electronics in the literature [6-8], but none on GA applied to multilevel inverters.

The rest of this paper is organized as follows. Section II is devoted to describing briefly the stepped waveform of a multilevel inverter's output voltage and its harmonic components. In Section III, the THD minimization strategy is explained, and then, it is applied to the phase voltage and line voltage of the inverter in Section IV, Section V deals with two sections of which the first one discuss the simulation for Cascaded inverter and section two discuss about simulation and results for diode clamped inverter followed by discussion and comparison of the THD values for both diode cascade and diode clamped multilevel inverters in Section VI. Finally, there is a conclusion in Section VII.

2. MULTILEVEL INVERTER'S OUTPUT VOLTAGE

Fig. 1 shows a half cycle of a typical stepped waveform of the phase voltage of a seven-level inverter with equal dc sources. The other half cycle is the same but in the opposite direction. V_{dc} is the dc source voltage of each H-bridge inverter, and assuming a symmetrical waveform, only three angles α_1, α_2, and α_3 are required to determine the whole cycle of the waveform. a_i, a_2, and a_3 are the switching angles of the three H-bridges, forming the seven-level inverter.

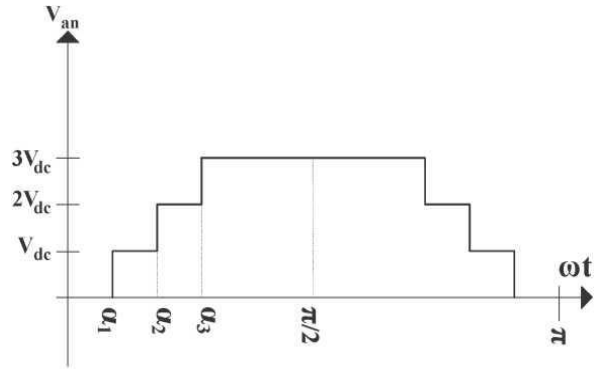

Fig. 1. Half cycle of the phase-voltage waveform

Fourier analysis of such a waveform yields the following expression for the rms value of fundamental and harmonic components of the phase voltage

$Vn = \frac{4\sqrt{2}}{n\pi} Vdc(\cos(n\alpha 1) + \cos(n\alpha 2) + \cos(n\alpha 3))$, *for odd n*
$= 0$, *for even n* -[1]

Because of quarter-wave symmetry in the waveform, it contains odd-order harmonics only. The maximum possible value of the fundamental component is obtained when $\alpha 1$, $\alpha 2$, and $\alpha 3$ are all equal to zero and is given by

$$V_1(max) = \frac{4\sqrt{2}}{\pi} V_{DC} \quad \text{- [2]}$$

Normalizing the fundamental component based on its maximum value and presenting it in per unit (p.u.)

$$\frac{V_1}{V_1(max)} = \frac{1}{3}(\cos(\alpha 1) + \cos(\alpha 2) + \cos(\alpha 3)) \quad \text{- [3]}$$

Considering the waveform in Fig. 1, the phase-voltage rms value can be easily calculated

$Vrms = Vdc \{\frac{2}{\pi}\{(\alpha 2 - \alpha 1) + 4(\alpha 3 - \alpha 1) + 9(\frac{\pi}{2} - \alpha 3)\}\}^{\frac{1}{2}}$ – [4]

The major problems associated with power quality now a days is total harmonic distortions (THD) and it is is defined as the ratio of all harmonic components' rms value to the fundamental component's rms value and is expressed as follows:

$$(THD)p = \sqrt{\left[\frac{\quad}{\quad}\right] - 1} \quad \text{-[5]}$$

3. LINE-VOLTAGE THD

Unlike the phase voltage, line-to-line voltage of the inverter has a waveform which is not as simple as that shown in Fig. 1, and depending on the values of switching angles, it changes the form. This is shown in Figs. 2 , where the line-voltage waveform is presented. As it is observed, the waveform has

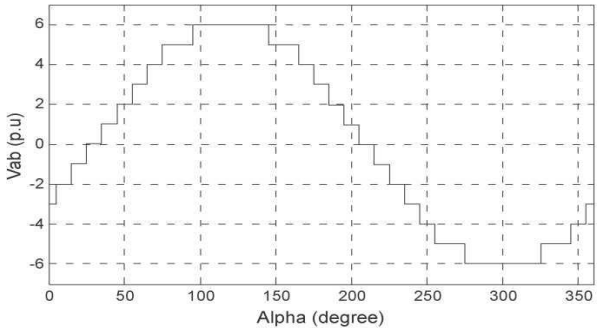

Fig. 2. Line-voltage waveform of the inverter with 13 levels

thirteen steps. Therefore, calculating its rms value is not straightforward, as for the phase voltage, and finding a unique analytical expression for the rms value is impossible for the entire range of the switching angles.

Instead, after having specified the waveform of the line voltage for any given values of switching angles, one can calculate its rms value by making use of the stepped waveform and integrating its rectangular segments.

Referring to the phase-voltage waveform shown in Fig. 1 and taking the phase voltage V_a as the phase reference, it can be expressed in terms of step function u(ut). The line voltage V_{ab} can now be obtained by subtracting V_b *from* V_a

$$Vab(ut) = Va(ut) - V_b(ut). \quad \text{–[6]}$$

Because of symmetry, the fundamental components of the phase voltages V_a and V_b have the same amplitude and 120° phase difference. Therefore, the rms value of the line-voltage fundamental component is $y/3$ times that of the fundamental component of the phase voltage

$$V_{L1} = \sqrt{3}V_1 = \frac{\sqrt[3]{6}\,Vdc}{\pi}\left(\cos(\alpha 1) + \cos(\alpha 2) + \cos(\alpha 3)\right) \quad \text{-[7]}$$

In per unit, based on its own possible maximum value, the line-voltage fundamental component is expressed by the same equation as

$$\frac{VL1}{VL1max} = \frac{1}{3}\left(\cos(\alpha 1) + \cos(\alpha 2) + \cos(\alpha 3)\right) \quad \text{-[8]}$$

Finally, THD of the line voltage is computed using the following equation $(THD)_L = \{[V_L/V_{L1}] - 1\}^2$ -[9]

4. THD MINIMIZATION

The aim is to determine the optimum switching angles that generate an output voltage with the required fundamental com-ponent and the possible minimum THD. This is a problem to be solved by an optimization algorithm. In this paper, GA is used which is a simple, powerful, and evolutionary technique, inspired from the laws of natural selection and genetics. It is a general-purpose stochastic global search algorithm, with no need of functional derivative information to search for the so-lutions that minimize (or maximize) a given objective function. GA reduces the computational burden and search time, while solving complex objective functions

To solve the problem for a given desired fundamental component $V\pm$ (in per unit), an objective function is defined as follows:

Objective Function : {10 $x(V^* - Vi)$ + THD} .

In the first term of the above mentioned objective function, $(V^* - V_i)$ is the absolute value of error in adjusting the fundamental component. A weighting factor of ten has been applied to make the error small enough, giving a greater importance to the fundamental component. The value of this factor can be controversial. Assigning a value of unity to the weighting factor results in the same weight for both the fundamental component's error and THD in the objective function. This means that the error in the fundamental component can be as much as the THD value. Typical values of the output THD, in the multilevel inverter under discussion, are mostly above 10%, i.e., 0.1 p.u., which is an unacceptable error for the fundamental component. To reduce the error to a level on the order of 1%, i.e., 0.01 p.u., a weighting factor of ten would be suitable. With the selected weighting factor, minimization of the objective function results in a fundamental component very close to the desired value as well as minimum THD in the voltage waveform. The solution must also satisfy the following constraint:

$$0 \le \alpha_1 \le \alpha_2 \le \alpha_3 \le \pi/2$$

The THD minimization algorithm may be applied either on the phase voltage or on the line-to-line voltage. Due to the simpler formulation, however, it is usually applied on the phase voltage. According to the selected approach (phase- or line-voltage THD minimization), the quantities in the objective function are substituted from the corresponding equations obtained in previous sections.

5.SIMULATIONS

5. 1 7- Level Cascaded Multilevel Inverter

The 3-phase, 7-level cascaded multilevel inverter consists of twelve switching devices, twelve main diodes and three DC bus capacitors as illustrated in Figure below. Here there is no clamping diodes connected. Three capacitors have been used to divide the DC link voltage into seven voltage levels thus the name of 7-level.

In this work, twelve switching devices are connected per leg. The switching signals should be synchronized with the AC supply voltage. Since the Matlab/Simulink does not have such triggering blockset, a new triggering block has been designed and developed using the blockset obtained from Simulink Toolbox. Also, the gate signals sequence and duration of conduction angle of the MOSFETs have been determined.

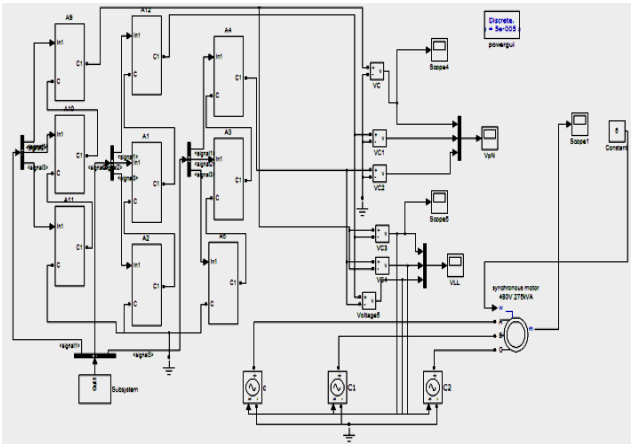

Fig 3: Simulink model of three phase 7 level cascaded H bridge inverter.

The corresponding phase voltage and line voltages are shown below. Fig 4 shows the phase voltage for all the three phases.

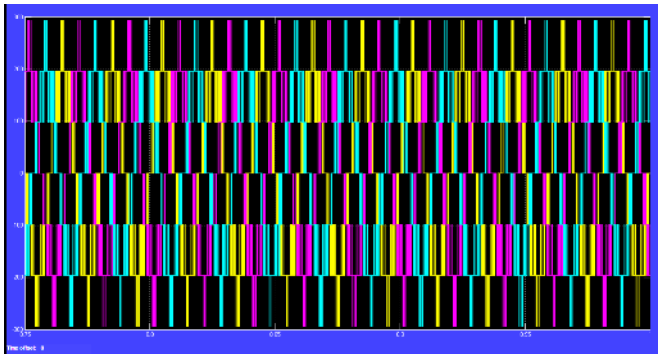

Fig 4: Phase Voltage (Van, Vbn, Vcn) of three phase 7-level CMLI

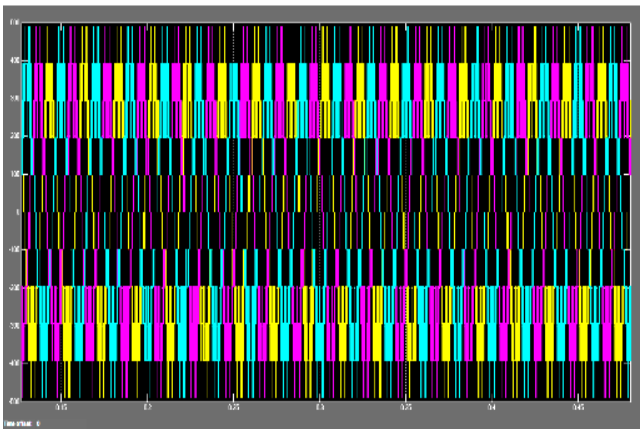

Fig 5: Line Voltages (Vab, Vbc, Vca) for 7 level CMLI

Fig 5 shows the Line voltage for all the three phases, ie Vab, Vbc, Vca. As shown in the simulation graph, the phase voltage value is 240 volts and that of line voltage is 470 volts.

FFT analysis for the seven level cascaded multilevel inverter for two cycles shown in fig 6 and fig 7 reveals the following datas. The phase voltage THD measured here is 19.44% and that of Line voltage is 15.23%

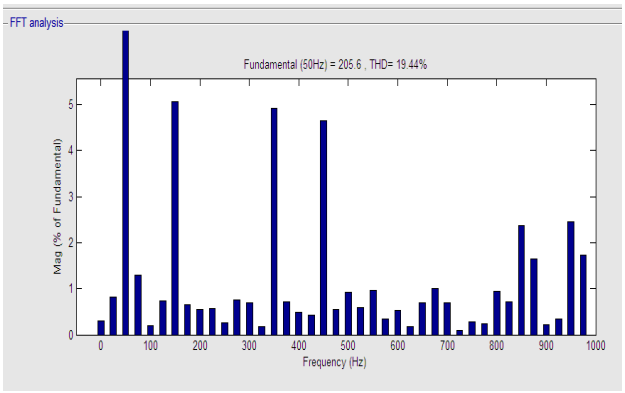

Fig 6: FFT analysis for phase voltage THD of 7 level inverter.

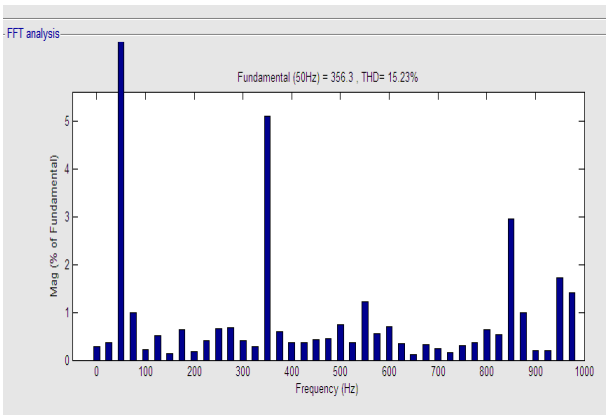

Fig 7: FFT analysis for line voltage THD of seven level inverter.

5. 2 9 Level Diode Clamped Multilevel inverter

In NPC multilevel inverters, the dc-link capacitors are series connected [1], [2] and will cause unequal voltage sharing between them the 3-phase, 9-level NPC multilevel inverter consists of 16 switches per leg, sixteen main diodes, fifty six clamping diodes and 8 DC bus capacitors as illustrated in Figure10. The clamping diodes are connected in such a way that it blocks the reverse voltage of the capacitor. Capacitors have been used to divide the DC link voltage into 9 voltage level thus the name of 9-level.

In this work, sixteen triggering signals are needed for the 3-level NPC inverter. These signals should be synchronized with the AC supply voltage. Since the Matlab/Simulink does not have such triggering blockset, a new triggering block has been designed and developed using the blockset obtained from Simulinifty six k Toolbox. Also, the gate signals sequence and duration of conduction angle of the MOSFETs have been determined. Fig 8 shows the simulation circuit for 9 level diode clamped multilevel inverter and fig 9 shows the subsystem for the simulation block.

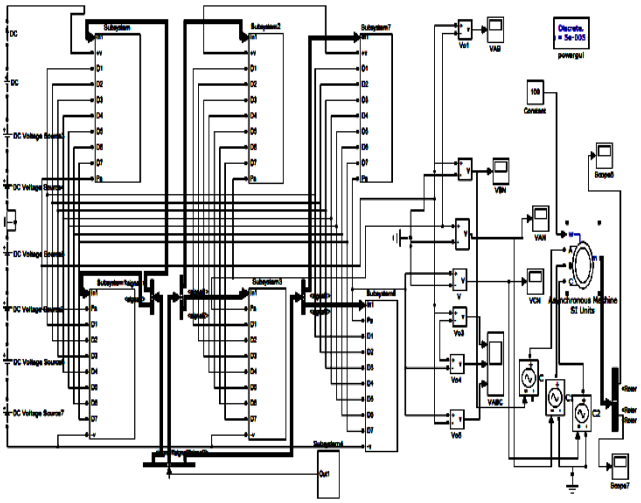

Fig 8: Simulink model for 9 level DCML inverter

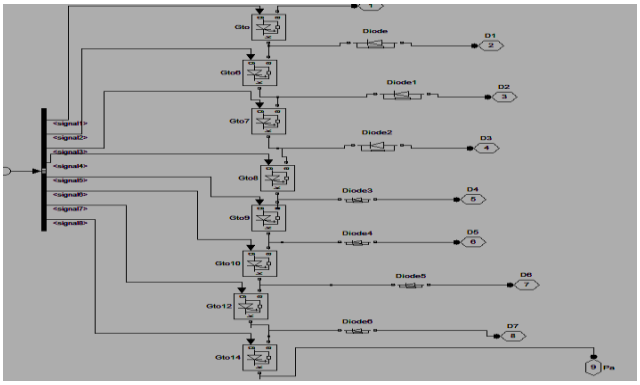

Fig 9: Output Phase Voltage (Van)of three phase 9-level DCMLI

The corresponding phase voltage and line voltages are

shown below. Fig 10 shows the phase voltage Van and fig 11 shows the Line voltage Vab for the 9 level diode clamped multi-level inverter.

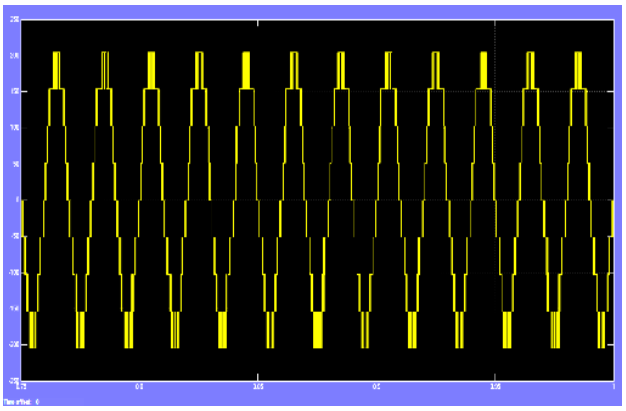

Fig 10: Phase voltage (Van) for 9 level DCML inverter

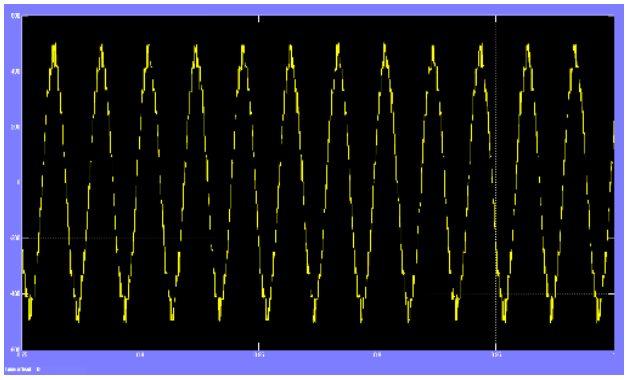

Fig 11: Line voltage (Van) for 9 level DCML inverter

As shown in the simulation graphs the phase voltage value is 240 volts and that of line voltage is 460 volts.

FFT analysis for the nine level cascaded multilevel inverter for two cycles shown in figure 12 and fig 13 reveals the following datas. The phase voltage THD measured here is 11.90% and that of Line voltage is 5.42 %

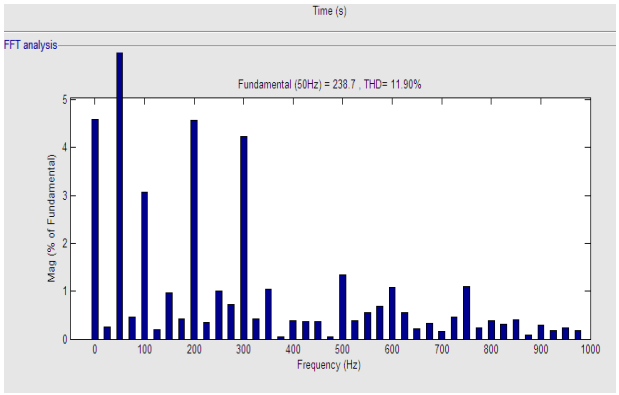

Fig 12: FFT analysis for phase voltage THD of 9 level DCML inverter

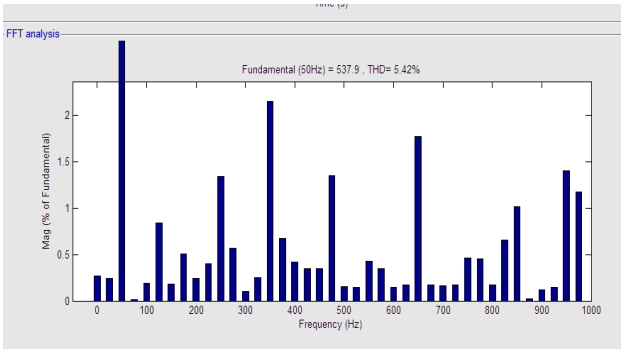

Fig 13: FFT analysis for line voltage THD of 9 level DCMLI

5. 3 COMPARISON CHART

A comparison chart is shown here which clearly shows the variation in THD values both in phase voltage and line voltages. Here the chart also justifies the statement that as level increases the THD value will normally decreases.

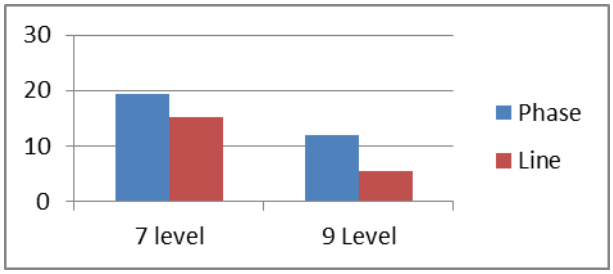

Fig 17 comparison between THD in line value and phase value.

5. 4 COMPARISON TABULATION.

A comparison tabulation is given below which clearly defines the numerical values for the THD values for both the simulations. In the case of cascaded MLI, a 4% reduction is there in line THD compared to the phase value. Later in Diode Clamped MLI, there will be 6% reduction in Line value than that of Phase. A reduction of 10% is there in the line value when the level steps up from seven to nine level.

Table 1: Comparison Table

Level of MLI	THD phase	THD line
7 CMLI	19.44%	15.23%
9 DCMLI	11.90%	5.42%

5. 5 COMPARISON BETWEEN TWO APPROACHES

Comparing the results of the two approaches indicates that they give different solutions. It indicates a significant improvement when the THD minimization algorithm is directly applied to the line voltage. In both cases, the optimum switching angles gen-

erate an output line-to-line voltage, the fundamental component of which very closely follows the desired value, but the THD contents are different. Within a wide range of the output voltages, the line-voltage THD minimization approach results in lower THD, with a reduction of up to 40%, compared to the phase-voltage THD minimization approach. The reason seems to be mostly the absence of triplen harmonics in the line voltage. Since the phase voltage contains all odd-order harmonics, including the triplens, its THD minimization gives the optimum condition for the phase voltage itself but not for the line voltage. To obtain the optimum condition for the line voltage, the harmonic components present at the line voltage should only be considered in the minimization process.

6. CONCLUSION

Till yet attention is mostly paid on phase voltages for the minimization of THD in multilevel inverters' output voltage, which has simpler waveform and easy formulation. Since, in three-phase applications, line-to-line voltage of the inverter is of the main concern, it is important to achieve as small THD as possible in the line voltage. Although phase-voltage THD minimization has a direct impact on the line-voltage THD, it does not necessarily lead to the possible minimum THD in the line voltage. It has been proposed in this paper to apply the THD minimization directly to the line voltage. By simulation results, the proposed approach has been shown to be more effective than the common approach of phase-voltage THD minimization and results in smaller THD in the line voltage. Also by considering the FFT for diode clamped multilevel inverter it clearly justifies the statement " THD minimizes as level increases" .The proposed system has many attractive features like, high voltage capability, reduced common mode voltages near sinusoidal outputs, lower value of dv/dt, smaller or even number output filters make multilevel inverter is a suitable topology for variable frequency induction motor drives and also been explored for low-voltage renewable grid interfacing applications.

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